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INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 6 : H01L 21/768, 23/532 — A1

(11) International Publication Number: **WO 99/63591**

(43) International Publication Date: 9 December 1999 (09.12.99)

(21) International Application Number: PCT/US99/11410

(22) International Filing Date: 26 May 1999 (26.05.99)

(30) Priority Data:

60/087,116	29 May 1998 (29.05.98)	US
09/149,910	9 September 1998 (09.09.98)	US

(81) Designated States: CA, CN, JP, European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE).

Published
With international search report.

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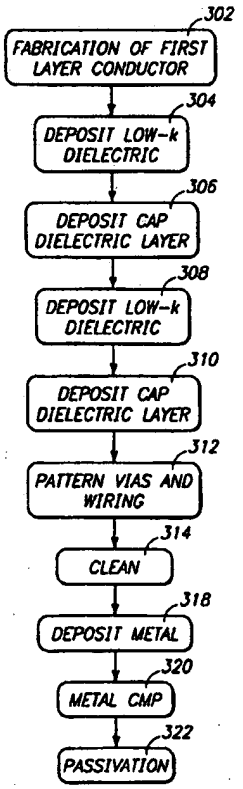
(54) Title: DUAL-DAMASCENE INTERCONNECT STRUCTURES EMPLOYING LOW-K DIELECTRIC MATERIALS

(57) Abstract

Interconnects in sub-micron and sub-half-micron integrated circuit devices are fabricated using a dual damascene process incorporating a low-k dielectric. A dual-damascene structure can be implemented without the necessity of building a single damascene base, and without CMP of the low-k dielectric. This structure simplifies the manufacturing process, reduces cost, and effectively reduces intra-level and inter-level capacitance, resistivity, and noise related to substrate coupling. In accordance with a further aspect of the present invention, a modified silicon oxide material such as silsesquioxane is used for the low-k dielectric in conjunction with silicon dioxide cap layers, allowing an improved process window and simplifying the etching process.



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DUAL-DAMASCENE INTERCONNECT STRUCTURES EMPLOYING LOW-K DIELECTRIC MATERIALS

TECHNICAL FIELD

The present invention relates, generally, to methods and structures for multilevel interconnects in integrated circuits using planarization technology and, more particularly, to a dual-damascene approach employing a low-k dielectric.

BACKGROUND ART AND TECHNICAL PROBLEMS

Advanced semiconductor processing technology has permitted the fabrication of integrated circuit devices with sub-micron and sub-half-micron features sizes. This trend toward deep submicron technology (i.e., involving feature sizes less than 0.35 microns) has, in turn, driven the need for multilayer interconnects. As a result, circuit performance in the deep submicron regime is increasingly a function of the delay time of electronic signals traveling between the millions of gates and transistors present on the typical integrated circuit chip. Parasitic capacitance and resistance effects resulting from these otherwise passive interconnect structures must therefore be well-controlled. Toward this end, recent trends emphasize the use of low resistance metals (e.g., copper) in conjunction with materials with low dielectric constants ("low-k dielectrics") between metal lines.

Optical lithography techniques have, for the most part, managed to keep pace with deep sub-micron requirements through the use of off-axis illumination, phase shifting masks, and other methods known in the art. However, the decreasing depth of focus that accompanies this increase in resolution requires the production of highly planar surfaces during intermediary process steps. In light of the need for highly planar surfaces, traditional metal deposition and photolithographic techniques become progressively more ineffective as line widths are scaled and multiple layers of metal are used. For example, traditional metal deposition techniques can result in poor metal step coverage along the edges of the contact openings. Furthermore, wet chemical etch processes typically used with metals are difficult to control. While dry

plasma etching may be employed with many metals, other metals with highly desirable properties (e.g., copper and gold) are generally not amenable to dry etching.

Modern semiconductor processing techniques increasingly employ Chemical-Mechanical Polishing (CMP) to create the interconnect layers, particularly where the number of layers rises above three and the conductive lines themselves are characterized by a high aspect ratio (e.g., lines on the order of 0.25 m in width and on the order of 1.0 m in height). In a paradigmatic CMP process, a resinous polishing pad (e.g., a polyurethane pad) is employed in conjunction with a mechanically and chemically active slurry. When pressure is applied between the polishing pad and the wafer being polished, mechanical stresses are concentrated on the exposed edges of the adjoining cells in the cellular pad. Abrasive particles within the slurry concentrated on these edges tend to create zones of localized stress at the workpiece in the vicinity of the exposed edges of the polishing pad. This localized pressure creates mechanical strain on the chemical bonds comprising the surface being polished, rendering the chemical bonds more susceptible to chemical attack by the slurry. Thus, with the correct choice of slurry, pressure, and other process conditions, a highly planar surface may be formed on the wafer. For additional information regarding CMP process, see, for example, *Karlsrud*, U.S. Patent No. 5,498,196, issued March, 1996; *Arai, et al.*, U.S. Patent No. 5,099,614, issued March, 1992; and *Arai, et al.*, U.S. Patent No. 4, 805,348, issued February, 1989. The entire contents of these references are hereby incorporated by reference.

A fabrication method which employs CMP techniques and which addresses many of the above concerns is the so-called "damascene" process. Damascening acquired its name from an ornamental technique, generally attributed to metal-workers in ancient Damascus, which involved scribing or incising patterns into steel (most often swords) then filling the resulting grooves with gold or silver prior to final polish. Similarly, the modern semiconductor analog of this process involves, in the broadest sense, forming patterns in a dielectric layer, filling the resulting pattern with interconnect metal, then polishing away the excess metal on the wafer surface and leaving inlaid interconnect metal.

There are two major classes of damascene processes: single-damascene and dual-damascene. These two processes are illustrated in highly simplified form in **Figures 1A and 1B** (details of the various intermediary steps are discussed in further detail below). Briefly, and with reference to **Figure 1A**, a single damascene process involves making contact to a lower conductor 102 (formed, for example, on substrate 107) by patterning and forming a conductive plug 104 in one layer of dielectric 106, then patterning second dielectric layer 110, and forming the actual interconnect wiring metallization 108 in patterned dielectric layer 110. In a dual-damascene process **(Figure 1B)**, the interconnect wiring 108 and plug 104 are formed by patterning both the via and the trench patterns into dielectric 106, then filling them simultaneously with metal. The dual damascene process offers the advantages of process simplification and low manufacturing cost.

Known methods of forming deep sub-half-micron damascene interconnect structures using low-k dielectrics are unsatisfactory in many respects. First, such methods typically employ a single-damascene approach. This results in a larger number of process steps -- a number which tends to increase as feature size decreases -- and, consequently, increases the overall product cost. In cases where a dual damascene architecture is employed, the low-k dual damascene processes typically require either a single damascene process as the starting point or CMP of the low-k material. In order to obtain the inlaid metal features with metal CMP, a damascene process requires a planar wafer surface. The first interconnect layers (e.g., poly-Si conductor layer or lower levels of Al interconnects) on an IC chip are typically fabricated by a subtractive-etch process, and CMP of the subsequently deposited dielectric must be performed in order to obtain a planar wafer surface.

To avoid CMP of the low-k material -- a process which is difficult to perform -- known low-k dual damascene processes start from a previous level of conductors fabricated by a single damascene process. Before the single damascene conductors are fabricated, a planar wafer surface is obtained by CMP of a conventional dielectric, such as silicon dioxide, and the contact or via plugs are formed in the conventional dielectric layer. However, the single damascene step results in relatively high process cost, and the conventional dielectric between the single damascene conductor layer

and the previous subtractive-etched conductor layer increases the capacitance and coupling between them.

Methods and structures are therefore needed in order to overcome these and other limitations in the prior art.

SUMMARY OF THE INVENTION

The above disadvantages of the prior art may be addressed by an improved dual-damascene process. Methods according to various aspects of the present invention provide techniques for fabricating IC interconnects using a dual-damascene process which incorporates a low-k dielectric material. In accordance with one aspect of the present invention, a low-k dual-damascene structure can be implemented without the necessity of using a previous single damascene wiring layer, and without CMP of the low-k dielectric. This structure simplifies the process, and effectively reduces intra-level and inter-level capacitance, reduces resistivity, and reduces noise related to substrate coupling. In accordance with a further aspect of the present invention, a modified silicon oxide material (e.g. silsesquioxane) is used for the low-k dielectric in conjunction with the silicon dioxide cap layers, allowing an improved process window and simplifying the etching process.

BRIEF DESCRIPTION OF THE DRAWING FIGURES

The subject invention will hereinafter be described in conjunction with the appended drawing figures, wherein like numerals denote like elements, and:

Figure 1A is a diagrammatic illustration of a conventional single damascene interconnect process;

Figure 1B is a diagrammatic illustration of a conventional dual-damascene interconnect process;

Figures 2A-2L depict cross-sectional views corresponding to an exemplary dual-damascene process in accordance with various aspects of the present invention; and

Figure 3 is a flowchart depicting an exemplary dual-damascene process in accordance with the present invention.

DETAILED DESCRIPTION OF PREFERRED EXEMPLARY EMBODIMENTS

An interconnect fabrication process in accordance with various aspects of the present invention utilizes a dual-damascene scheme incorporating a low-k inter/intra-level dielectric material. With momentary reference to **Figure 2I**, a simplified dual-damascene process employs low-k dielectric layers 208 and 212 in conjunction with cap dielectric layers 210 and 214 to form an interconnect metal structure 220 with reduced intralevel and interlevel capacitance. In accordance with an illustrated embodiment, a dual-damascene structure can be implemented without the necessity of using previous single damascene wiring layer, and without CMP of the low-k dielectric.

Referring now to **Figures 3 and 2A-2L**, an interconnect fabrication process in accordance with various aspects of the present invention will now be described in detail. It should be understood that the exemplary process illustrated may include more or less steps or may be performed in the context of a larger processing scheme.

Prior to performing the dual damascene process steps, a first metal layer 204 and dielectric 206 are initially formed on substrate 202 as shown in **Figure 2D**. In a preferred embodiment, and as described further below, a thin layer of dielectric material is left remaining on top of metal layer 204. This structure, which helps achieve the objects of the present invention, may be formed in a variety of ways. In the illustrated embodiment, processing takes place as depicted in **Figures 2A-2C**.

Specifically, a metal layer 204 (or, more generally, a conductor) is deposited on substrate 202 and patterned using conventional techniques, for example, through sputter deposition followed by photolithography and plasma etching (**Figure 2A**). Metal layer 204 suitably comprises a layer or layers of metal (e.g., aluminum, aluminum alloys, titanium, titanium nitride, tantalum, tantalum nitride, gold, copper, copper alloys, molybdenum, silver, tungsten, etc.), polycrystalline silicon ("polysilicon"), or a variety of other conductive materials.

Next, a dielectric 206 is deposited for gap fill; i.e., to fill gaps within the patterned conductor layer 204 (**Figure 2B**). Dielectric 206 suitably comprises a layer or layers of silicon dioxide (doped or undoped), silicon nitride, silicon oxynitride, or a variety of other substantially non-conductive materials. In the illustrated exemplary

embodiment, dielectric 206 used for gap fill comprises a layer of high-density plasma (HDP) chemical vapor deposition (CVD) silicon dioxide. A suitable thickness of this layer is approximately 0.5-1.0 microns. Other gap fill techniques, such as PECVD deposit-etch-deposit technique may be employed.

As shown in **Figure 2C** a second dielectric layer 207 is then preferably deposited on top of layer 206 using conventional CVD techniques, for example, plasma-enhanced chemical vapor deposition (PECVD). This layer, which is preferably about 0.4 - 1.0 microns, is then planarized and polished back using CMP such that a thin layer of dielectric 205 approximately 0.1 microns thick remains above metal 204. Alternatively, all of dielectric material 205 may be removed from the top of metal 204.

Substrate 202 consists of any suitable structure or material upon which or within which semiconductor devices are formed. Suitable materials include, for example, group IV semiconductors (i.e., Si, Ge, and SiGe), group III-V semiconductors (i.e., GaAs, InAs, and AlGaAs), and other less-conventional materials, such as SiC, diamond, and sapphire. Substrate 202 may comprise single crystal material, or may comprise one or more polycrystalline or amorphous epitaxial layer formed on a suitable base material. It will be appreciated that substrate 202 may also comprise various devices incorporated into a semiconductor material as well as interconnect structures consisting of conductive paths and various dielectrics for isolating these conductive paths.

Referring now to **Figure 2E**, after fabrication of the first layer conductor, a low-k dielectric layer 208 is deposited (Step 304). Generally, a low-k dielectric is a dielectric material which exhibits a dielectric constant substantially less than conventional dielectric materials such as silicon dioxide, silicon nitride, and silicon oxynitride. Silicon dioxide, for example, has a dielectric constant of about 4.0.

Dielectric 208 therefore suitably comprises one or more layers of inorganic, organic, or hybrid inorganic-organic low-k materials. In a preferred embodiment, dielectric layer 208 comprises a silsesquioxane monomer having a thickness of about 0.4 - 0.8 microns. Suitable silsesquioxanes include, for example, hydrogen silsesquioxane (HSQ) and methylsilsesquioxane (MSQ). Such materials have been found to exhibit dielectric constants in the range of about 2.2 to 3.2. Layer 208 is

suitably formed using a conventional spin-on process followed by a standard curing step of the kind well known in the art. In general, low-k dielectric preferably comprises a material with a chemical structure similar to that of silicon dioxide, for example, porous silicon oxide (e.g., aerogel or xerogel formed through an appropriate spin-on process followed by suitable curing) and fluorinated silicon oxide (formed through a PCVD process). Such materials have been found to exhibit dielectric constants in the range of about 1.2 to 3.8.

In Step 306, a cap dielectric layer 210 is formed over low-k dielectric layer 208. In a preferred embodiment, layer 210 comprises a PECVD layer of silicon dioxide approximately 0.1 - 0.3 microns thick, although other cap materials and thicknesses are suitable.

In Steps 308 and 310, a second low-k dielectric layer 212 and second cap dielectric layer 214 are formed as detailed above in connection with Steps 304 and 306. It should be appreciated that layers 212 and 214 may be formed with thicknesses differing from layers 208 and 210 respectively. The present invention is not limited to the case where the layer materials and thicknesses are the same.

Referring now to **Figure 2F and 2G**, the desired wiring and via patterns are formed in layers 208, 210, 212, and 214, as well as the thin oxide layer 205 above conductor 204 (Step 312). In an exemplary embodiment, this step involves forming trenches 216 (**Figure 2F**) and vias 218 (**Figure 2G**) using a trench-first dual-damascene process. Alternatively, a via-first process may be employed to fabricate trenches 216 and vias 218. The task of transferring the interconnect vias and wiring pattern into low-k dielectric layers 208 and 212 is suitably accomplished using conventional dual-damascene patterning techniques. See, for example, J. G. RYAN ET AL., ADVANCED METALLIZATION AND INTERCONNECT SYSTEMS FOR ULSI APPLICATIONS IN 1997, p. 399 (Sep. 30-Oct. 2, 1997); and P. Singer, SEMICONDUCTOR INTERNATIONAL, vol. 20, no. 9, p. 79 (Aug. 1997). In a preferred embodiment, fluorocarbon based chemistries are used for etching both the oxide cap layers and low-k layers, thereby reducing process complexity.

During Step 312, cap layer 210 between the two low-k layers serves as an etch buffer for the low-k dielectric etch to form the trench. Both top cap layer 214 and

middle cap layer 210 serve as protection layers for the photoresist strip. Under conventional plasma etch conditions for silicon dioxide, a preferred low-k material (i.e., silsesquioxane) exhibits an etch rate approximately twice that of silicon dioxide. For additional information regarding etching of silicon dioxide, silicon nitride, and the like, see, for example, Givens et al., *Selective dry etching in a high density plasma for 0.5 m complementary metal-oxide-semiconductor technology*, J. VAC. SCI. TECHNOL. B, p. 427 (Jan/Feb 1994). The low-k material is suitably etched in gas mixtures of a type used for silicon dioxide, thereby greatly simplifying etch-tool configurations and chemistry employed.

Patterning Step 312 is suitably performed in conjunction with various known lithographic techniques, for example, conventional optical lithography (including, for example, I-line and deep-UV), X-ray, or E-beam lithography. After patterning in Step 312, a cleaning step such as sputter clean or reactive gas clean may be employed in order to prepare the surfaces for further processing (Step 314).

In Step 318, one or more metal layers are formed. Depending on the particular process, a suitable adhesion/wetting/barrier metal layer may be deposited within trenches 216 and vias 218. As is known in the art, adhesion layers generally assist in strengthening the bond between metal and dielectric layers, and barrier layers provide a barrier to prevent the migration or alloying of one material into another (for example, copper diffusion into silicon). Wetting layers promote metal fill in high aspect-ratio features. In this regard, it should be appreciated that a single material may exhibit one or more of these properties in a particular context. Thus, the terms "adhesion layer", "wetting layer", and "barrier layer" as used herein are not meant to be limiting.

The adhesion/wetting/barrier layer (not shown in **Figure 2**) may consist of a variety of materials, for example, titanium, titanium nitride, tantalum, tantalum nitride, tungsten nitride, TiSiN, TaSiN, CoWP, tungsten, and/or molybdenum. In an exemplary embodiment involving aluminum metallization, a thin Ti wetting layer approximately 25-50 nm thick is deposited at 20 degrees Celsius through Hollow Cathode Magnetron (HCM) sputtering. Such systems are known in the art. See, for example, U. S. Pat. No. 5,482,611, issued to Helmer et al. Alternatively, collimated Ti deposition may be employed. In an embodiment using a copper metallization scheme, an

adhesion/barrier layer suitably comprises a Ta and/or TaN film deposited using ionized metal plasma (IMP) sputtering at a temperature less than approximately 350 C.

Referring now to **Figure 2H**, Step 318 involves depositing bulk metal 220 within the previously formed vias and trenches such that metal 220 makes electrical contact with first level metal (or conductor) 204. Metal 220 suitably consists of a layer or layers of various conductive materials, including, for example, titanium, titanium nitride, tantalum, tantalum nitride, tungsten nitride, aluminum, aluminum-copper alloys, gold, copper, silver, tungsten, or any other suitable conductive material. It will be appreciated that use of the term "interconnect metal" does not limit the present invention to metallic interconnects; other suitable conductors, for example, polysilicon, may be employed.

Deposition of metal 220 may be performed using a variety techniques. In a first embodiment, metal 220 comprises Al-Cu(0.5%) deposited using a low pressure sputtering process at a pressure of about 0.6 mTorr and a wafer temperature of about 400 degrees Celsius. The thickness of metal 220 in this embodiment is suitably 1.2-2.0 microns thick, although other metal thicknesses may be used. In addition to low-pressure sputtering, HCM sputtering, and any suitable combination of PVD and CVD metal deposition techniques may be employed.

In an alternate embodiment, metal 220 comprises copper deposited using electrochemical deposition (or "electroplating"). Copper is desirable in that its conductivity is relatively high and it is less susceptible to electromigration failure than many metals (for example, aluminum). Many commercial tools are suitable for this copper-forming step, including, for example, the EQUINOX tool manufactured by Semitool and the SABRE tool manufactured by Novellus. Such a system suitably employs a $CuSO_4$-based bath at room temperature using a DC/pulse current waveform control. Alternatively, conventional CVD and/or high-temperature PVD processes may be employed for copper deposition. In a preferred embodiment, a barrier layer and a copper seed layer are deposited prior to forming bulk copper layer 220. The seed layer helps in delivering electron current uniformly on the wafer for initiation of copper plating. The barrier and copper seed layers are suitably formed using IMP or HCM

sputtering deposition for better bottom and sidewall coverage. Alternatively, the barrier and copper seed layers may be deposited using CVD.

In Step 320, the excess metal 220 and corresponding adhesion/wetting/barrier layers on the field are removed, forming a substantially planar top surface (**Figure 2I**). In an exemplary embodiment, this planarization step is performed using a conventional CMP process. In the aluminum metallization context, a suitable CMP slurry comprises a mixture of hydrogen peroxide and an alumina abrasive used in conjunction with a polyurethane-based pad such as any of the IC1000 pads manufactured by Rodel.

A suitable slurry for copper CMP consists of any one of the following combinations: hydrogen peroxide and alumina; ammonium hydroxide and alumina; or nitric acid and alumina. This process can be performed using a conventional polyurethane pad, for example, the IC1000 and IC1400 pads manufactured by Rodel. During the CMP process, layer 214 serves as a CMP-stop layer to protect the low-k film.

In Step 322, a passivation layer 222 is formed over the planarized surface as shown in **Figure 2I**. Passivation layer 222 preferably comprises silicon dioxide, silicon nitride, or silicon oxynitride formed using conventional processing techniques such as PECVD. In the case where metal 220 is copper, silicon nitride is preferably used as at least a barrier layer to prevent copper diffusion.

Thus, upon completion of Step 322, a dual-damascene structure has been advantageously formed within the low-k material layers. It will be appreciated that multiple interconnect levels may be fabricated using methods in accordance with the present invention. More particularly, as shown in **Figures 2J-2L**, it is possible to repeat Steps 304-322 to form subsequent dual damascene structures -- for example, by depositing metal 234 within trenches 228 and vias 232 formed within low-k dielectric layers 230 and 224 respectively.

Although the invention has been described herein in conjunction with the appended drawings, those skilled in the art will appreciate that the scope of the invention is not so limited. Various modifications in the selection, design, and arrangement of the various components and steps discussed herein may be made without departing from the scope of the invention.

CLAIMS

What is claimed is:

1. A method for forming an interconnect in an integrated circuit device, said method comprising the steps of:

(a) providing a substantially planar layer comprising a conductor and gap-fill dielectric;

(b) forming a first low-k dielectric layer on said conductor and gap-fill dielectric;

(c) forming a first cap dielectric layer over said first low-k dielectric layer;

(d) forming a second low-k dielectric layer on said first cap dielectric layer;

(e) forming a second cap dielectric layer over said second low-k dielectric layer;

(f) patterning said first and second low-k dielectric layers and said first and second cap dielectric layers to form vias and trenches, wherein said vias are formed in said first low-k dielectric layer and said trenches are formed in said second low-k dielectric layer, and wherein said first cap dielectric layer acts as an etch buffer during patterning;

(g) forming a metal layer over said second cap dielectric layer and within said vias and said trenches such that said metal layer is electrically continuous with said conductor;

(h) removing excess regions of said metal layer from said second cap dielectric layer to form a substantially planar surface.

2. The method of claim 1, wherein said steps of forming said first and second low-k dielectric layers comprise the step of depositing a modified silicon oxide layer.

3. The method of claim 2, wherein said step of depositing a modified silicon oxide layer comprises the step of depositing a layer of silsesquioxane.

4. The method of claim 1, wherein said steps of forming said first and second low-k dielectric layers comprise the step of depositing a porous silicon dioxide layer.

5. The method of claim 1, wherein said steps of forming said first and second low-k dielectric layers comprise the step of depositing a fluorinated silicon oxide layer.

6. The method of claim 1, wherein said step of forming a metal layer comprises the step of depositing a layer of aluminum.

7. The method of claim 1, wherein said step of forming a metal layer comprises the step of depositing a layer of Al-Cu(0.5%).

8. The method of claim 7, wherein said Al-Cu(0.5%) is deposited using low-pressure sputtering, HCM sputtering, IMP sputtering, CVD, or a combination of CVD and PVD deposition.

9. The method of claim 1, wherein said step of forming a metal layer comprises the step of depositing a bulk layer of copper.

10. The method of claim 9, wherein said copper is deposited using electrochemical deposition.

11. The method of claim 9, further comprising the step of depositing a copper seed layer within said trenches and said vias prior to said step of depositing said bulk layer of copper.

12. The method of claim 1, further comprising the step of depositing a barrier layer, an adhesion layer, or a wetting layer within said trenches and said vias.

13. The method of claim 1, wherein said steps of forming said first and second cap dielectric layers comprises the step of depositing a layer of silicon dioxide.

14. The method of claim 1, wherein said step of providing a substantially planar layer comprises the steps of:

depositing and patterning said conductor;

forming a gap-fill dielectric layer over said conductor;

forming a second dielectric layer over said gap-fill layer; and

planarizing said gap-fill dielectric layer and said second dielectric layer such that a thin layer of dielectric remains over said conductor.

15. The method of claim 1, wherein said patterning step comprises the step of performing a via-first patterning process.

16. The method of claim 1, wherein said patterning step comprises the step of performing a trench-first patterning process.

17. An interconnect structure for connecting to a conductor in an integrated circuit device, said interconnect structure comprising:

a substantially planar first level conductor layer comprising a conductor and gap-fill dielectric;

a first low-k dielectric layer formed on said first level conductor layer;

a first cap dielectric layer formed over said first low-k dielectric layer;

a second low-k dielectric layer formed on said first cap dielectric layer;

a second cap dielectric layer formed over said second low-k dielectric layer;

a via formed in said first low-k dielectric layer and a trench communicating with said via formed in said second low-k dielectric layer;

a metal layer formed within said via and said trench such that said metal layer is electrically continuous with said conductor, and wherein said metal layer and said second cap dielectric layer are substantially planar.

18. The interconnect structure of claim 17, wherein said first and second low-k dielectric layers comprise a modified silicon oxide layer.

19. The interconnect structure of claim 17, wherein said first and second low-k dielectric layers comprise a porous silicon dioxide layer.

20. The interconnect structure of claim 17, wherein said first and second low-k dielectric layers comprise a fluorinated silicon oxide layer.

21. The interconnect structure of claim 18, wherein said modified silicon oxide layer comprises a layer of silsesquioxane.

22. The interconnect structure of claim 17, wherein said metal layer comprises a layer of aluminum.

23. The interconnect structure of claim 17, wherein said metal layer comprises a layer of Al-Cu(0.5%).

24. The interconnect structure of claim 17, wherein said metal layer comprises a layer of copper.

25. The interconnect structure of claim 24, wherein said metal layer further comprises a copper seed layer and a barrier layer.

26. The interconnect structure of claim 17, wherein said first and second cap dielectric layers comprise a layer of silicon dioxide.

27. The interconnect structure of claim 17, wherein said metal layer comprises a barrier layer, an adhesion layer, or a wetting layer.

28. The interconnect structure of claim 17, wherein said conductor comprises a polysilicon conductor.

29. The interconnect structure of claim 17, wherein said substantially planar first level conductor layer comprises a conductor, a gap-fill dielectric, and a thin dielectric layer covering said gap-fill dielectric and a portion of said conductor.

30. An interconnect structure for connecting to a conductor in an integrated circuit device, said interconnect structure comprising:

a dual-damascene metal structure formed in a low-k dielectric, wherein said dual-damascene metal structure is electrically continuous with said conductor;

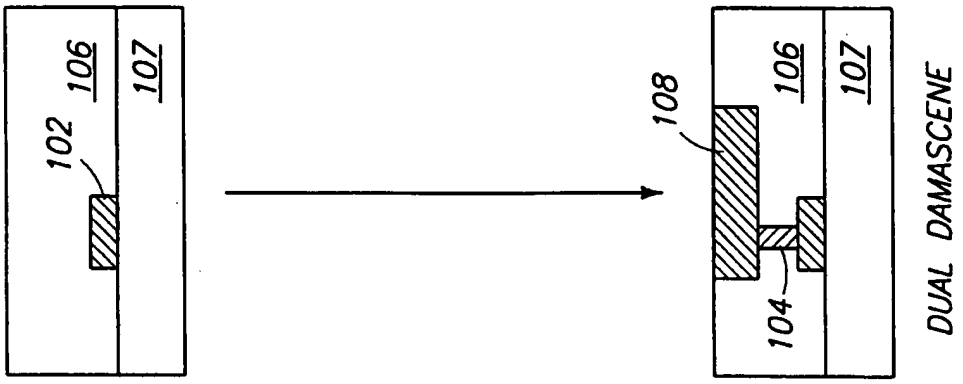
said low-k dielectric being formed over a substantially planar first level conductor layer comprising a conductor, a bulk dielectric, and a gap-fill dielectric layer.

31. The interconnect structure of claim 30, wherein said low-k dielectric comprises a modified silicon oxide layer.

32. The interconnect structure of claim 30, wherein said low-k dielectric comprises a modified silicon oxide layer.

33. The interconnect structure of claim 30, wherein said low-k dielectric comprises a modified silicon oxide layer.

34. The interconnect structure of claim 30, wherein said conductor comprises a polysilicon conductor.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DUAL DAMASCENE

FIG. 1B

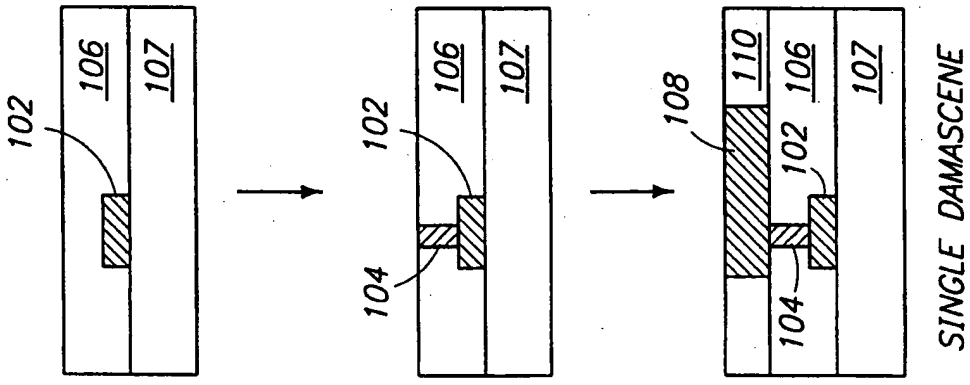
102
106
107
104
108
110
SINGLE DAMASCENE

FIG. 1A

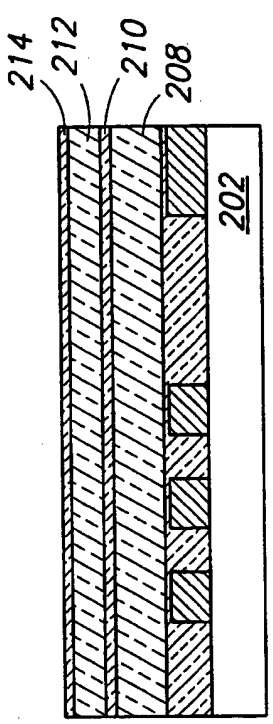

FIG. 2E

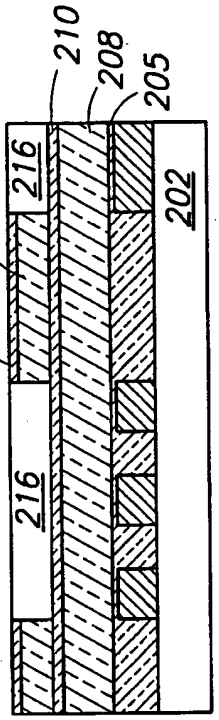

FIG. 2F

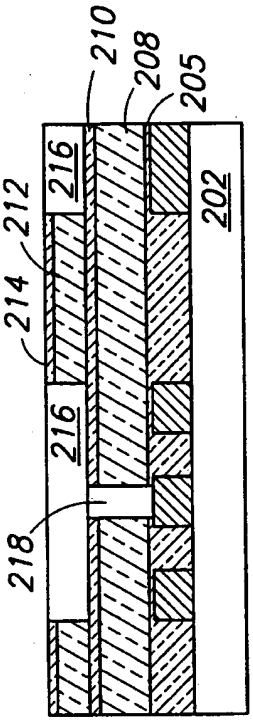

FIG. 2G

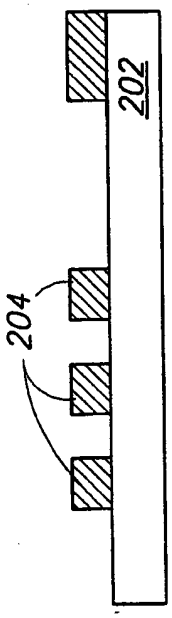

FIG. 2A

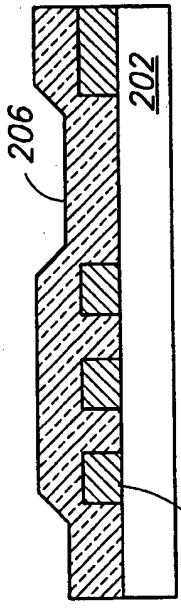

FIG. 2B

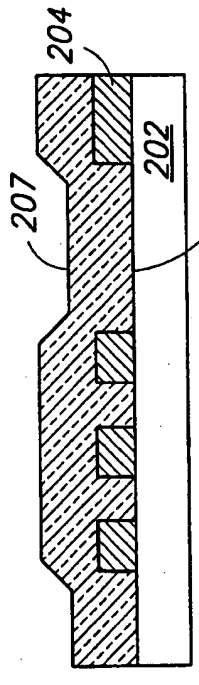

FIG. 2C

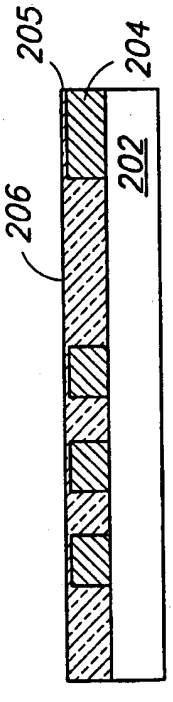

FIG. 2D

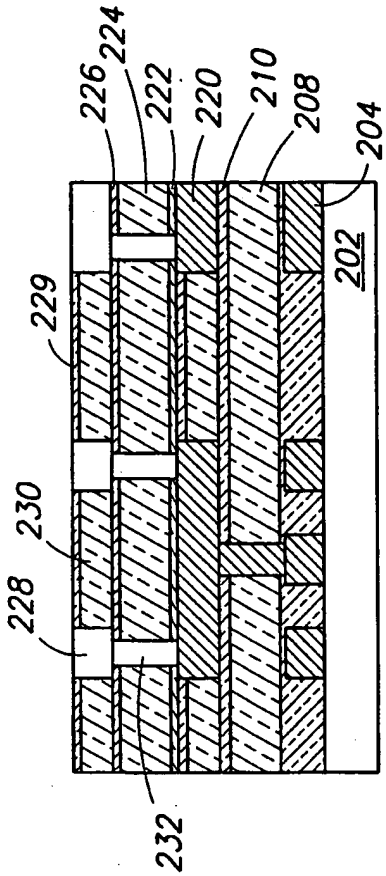

FIG. 2K

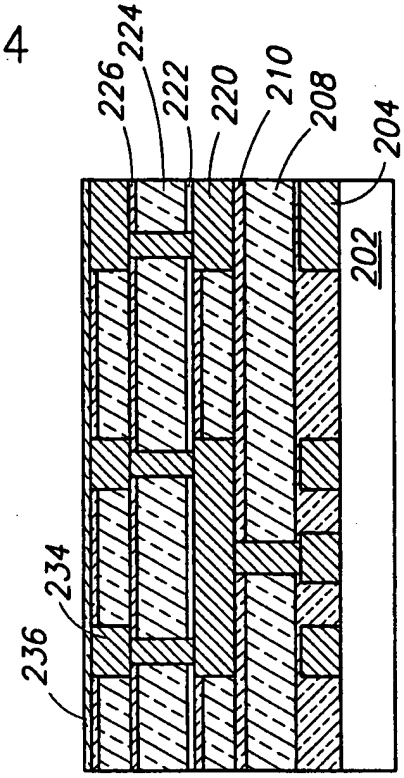

FIG. 2L

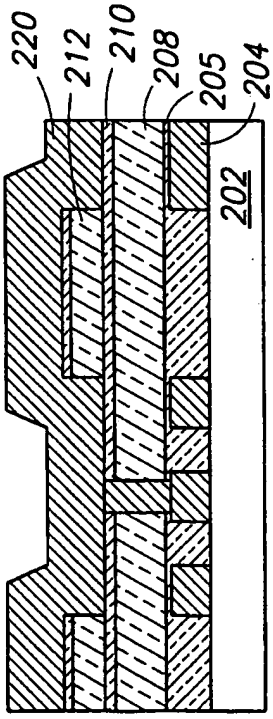

FIG. 2H

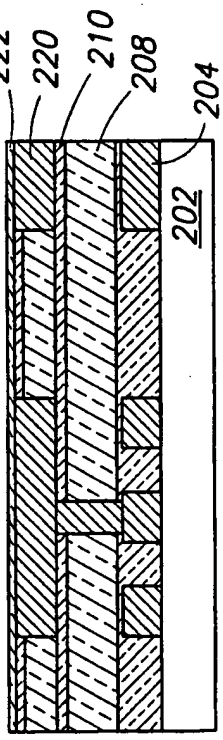

FIG. 2I

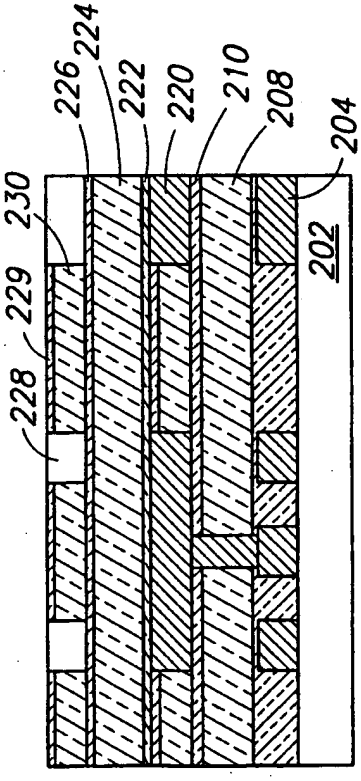

FIG. 2J

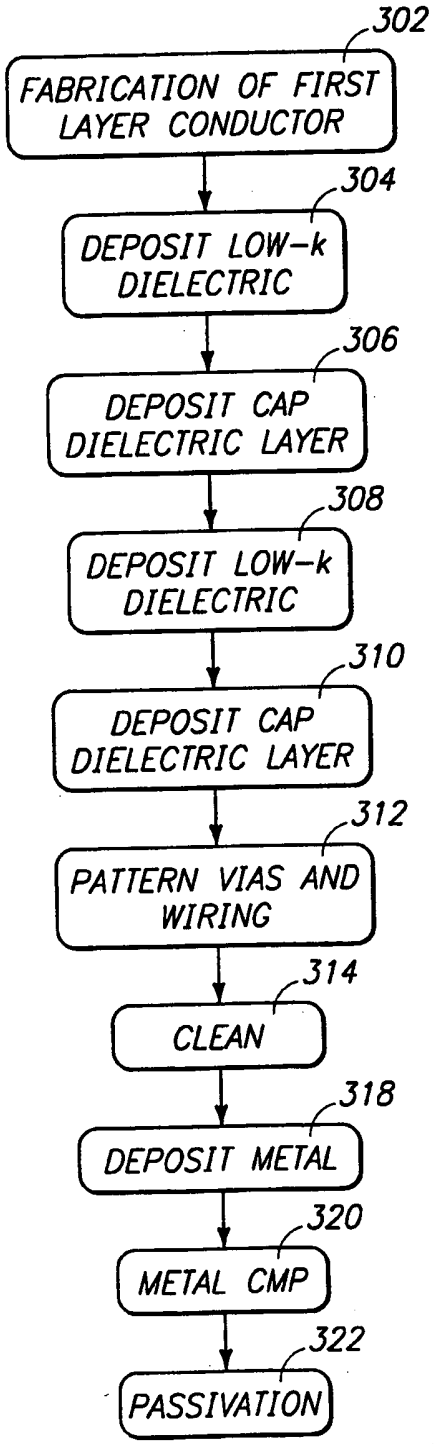
302
FABRICATION OF FIRST LAYER CONDUCTOR
304
DEPOSIT LOW-k DIELECTRIC
306
DEPOSIT CAP DIELECTRIC LAYER
308
DEPOSIT LOW-k DIELECTRIC
310
DEPOSIT CAP DIELECTRIC LAYER
312
PATTERN VIAS AND WIRING
314
CLEAN
318
DEPOSIT METAL
320
METAL CMP
322
PASSIVATION

FIG. 3

INTERNATIONAL SEARCH REPORT

	National Application No PCT/US 99/11410

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 H01L21/768 H01L23/532

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5 741 626 A (JAIN AJAY ET AL) 21 April 1998 (1998-04-21) column 2, line 31 - line 46 column 2, line 53 - line 58 column 2, line 67 - column 3, line 2 column 3, line 4 - line 8 column 3, line 9 - column 4, line 51 column 5, line 17 - column 6, line 25 figures 1-5,9-12	1-34
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[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

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"O" document referring to an oral disclosure, use, exhibition or other means

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
2 September 1999	14/09/1999

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Munnix, S

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INTERNATIONAL SEARCH REPORT

national Application No
PCT/US 99/11410

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
A	PATENT ABSTRACTS OF JAPAN vol. 096, no. 007, 31 July 1996 (1996-07-31) & JP 08 064595 A (FUJITSU LTD), 8 March 1996 (1996-03-08) abstract	1,5,13, 20,26
A	US 5 521 424 A (UENO KAZUYOSHI ET AL) 28 May 1996 (1996-05-28) abstract column 1, line 6 - line 21 column 4, line 21 - line 62 figure 2	1,5,13, 20,26
A	US 5 593 741 A (IKEDA YASUO) 14 January 1997 (1997-01-14) column 3, line 45 - line 51 column 7, line 65 - column 8, line 25 figure 6	1,14,17, 29,30
A	EP 0 731 503 A (TEXAS INSTRUMENTS INC) 11 September 1996 (1996-09-11) column 3, line 12 - line 24 column 3, line 35 - line 47 column 3, line 55 - line 56 claims 4-6,11,13,15	2,3,6-9, 11,12, 18, 21-25, 27,31-33
A	EP 0 793 268 A (TEXAS INSTRUMENTS INC) 3 September 1997 (1997-09-03) abstract column 3, line 2 - column 5, line 3 claim 12	2,3,6-9, 11,12, 18, 21-24, 27,31-33
A	US 5 256 274 A (PORIS JAIME) 26 October 1993 (1993-10-26) column 6, line 26 - column 7, line 47	9-12,24, 25
A	P. SINGER: "Making the Move to Dual Damascene Processing" SEMICONDUCTOR INTERNATIONAL, vol. 20, no. 9, August 1997 (1997-08), pages 79-82, XP002114089 cited in the application figures 1-3	15,16

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INTERNATIONAL SEARCH REPORT

national Application No
PCT/US 99/11410

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

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A	J.G. RYAN ET AL.: "Technology Challenges for Advanced Interconnects" CONFERENCE PROCEEDINGS ULSI XIII, 30 September 1997 (1997-09-30) - 2 October 1997 (1997-10-02), pages 399-404, XP002114090 cited in the application the whole document	1-34

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INTERNATIONAL SEARCH REPORT

Information on patent family members

National Application No
PCT/US 99/11410

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JP 02126639 A	15-05-1990	NONE	